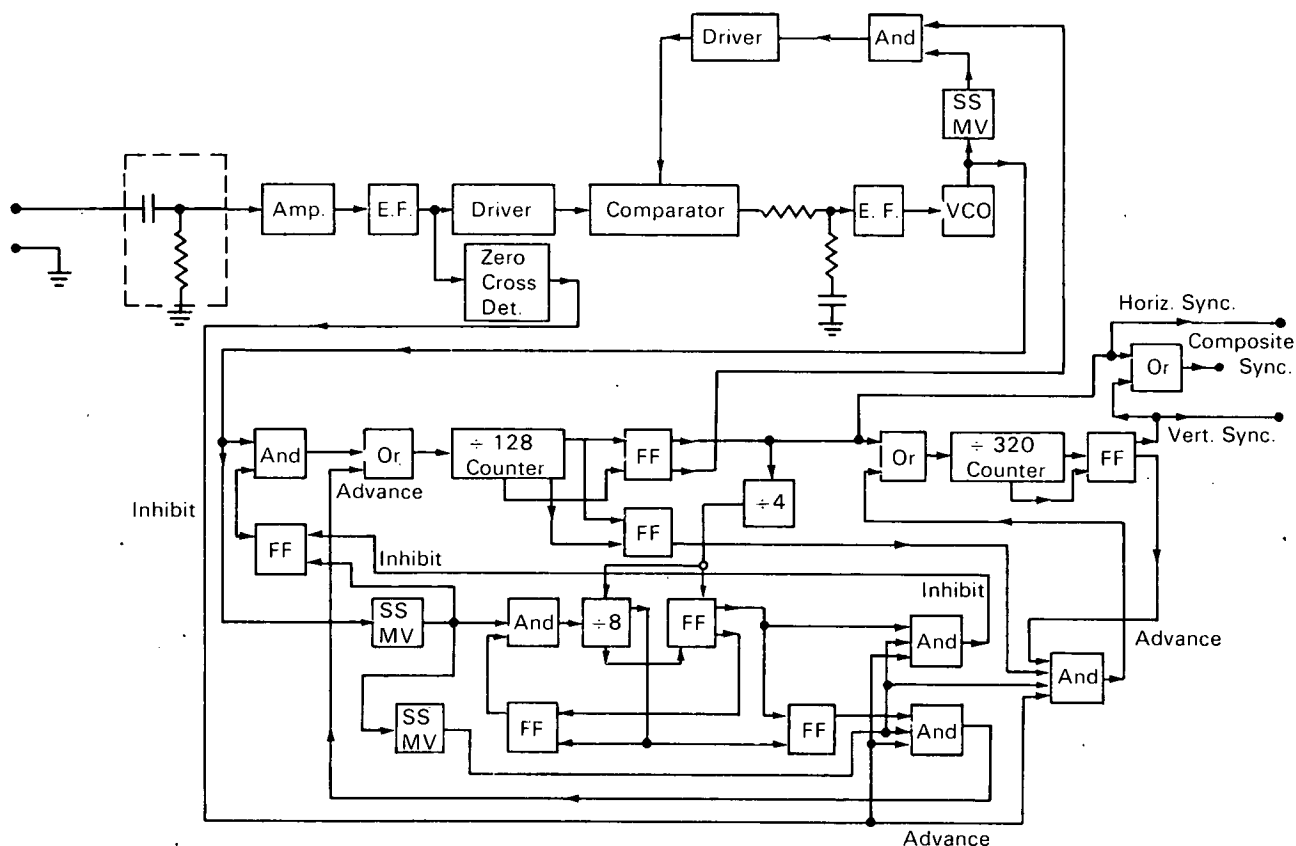


# NASA TECH BRIEF



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## Burst Synchronization Detection System



The burst synchronization detection system was developed for use with long-range, slow-scan television units. The detection system separates synchronizing bursts from the remainder of the incoming signals and supplies such bursts to a phase-lock loop, that locks a voltage-controlled oscillator in the loop in synchronism with the sine wave component of the synchronizing bursts. Pulse signals from the oscillator

are supplied to a first-pulse counter to produce horizontal sync pulses with the same repetition rate as the sync bursts. The horizontal sync pulses are supplied to a second pulse counter to produce vertical sync pulses with the same repetition rate as the vertical sync intervals in the incoming signal.

A first comparison circuit compares the horizontal sync pulses with the oscillator signal and the incoming

(continued overleaf)

sync bursts to pull the horizontal sync pulses into phase with the sync bursts. A second comparison circuit compares the vertical sync pulses with the oscillator signal and the incoming sync bursts to pull the vertical sync pulses into phase with the vertical sync intervals of the incoming signal.

A circuit diagram, partly schematic, of the burst synchronization detection system is shown in the figure.

This invention is novel in that it uses digital logic in conjunction with a voltage-controlled oscillator to obtain appropriate horizontal and vertical sync signals from the sync bursts contained in the original transmitted signal. It would be useful in a system that exhibited considerable single amplitude fluctuation in overcoming the limitations of band-pass filtering, i.e., long response times.

**Notes:**

1. This invention may be of interest to designers and manufacturers of portable and mobile communication equipment.

2. Requests for further information may be directed to:

Technology Utilization Officer  
Manned Spacecraft Center, Code BM7  
Houston, Texas 77058  
Reference: TSP70-10159

**Patent status:**

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Source: Bryant P. Seay, Jr., NASA/MSC and  
Phillip C. Lipoma of  
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